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10/596,249	06/06/2006	Frederick William Buehrer	FIS920030120US1	4225

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EXAMINER	
SARKAR, ASOK K	

ART UNIT	PAPER NUMBER
2891	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/596,249	BUEHRER ET AL.	
	Examiner	Art Unit	
	Asok K. Sarkar	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 June 2006 and 08 July 2009* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 – 6, 14 – 18 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Guldi, US 5,525,529.

Regarding claim 1, Guldi teaches a method for selectively modifying a diffusions rate of an impurity implanted in a semiconductor material including steps of

- defining a boundary with a structure on a surface of said semiconductor material with reference to Fig. 3;
- applying a stressed film 58 over said structure and said surface at said boundary with reference to Fig. 3; and
- annealing said semiconductor material to activate said impurities, wherein said diffusion rate of said impurity is modified in both lateral and vertical directions in a region of said semiconductor material adjacent to said boundary after said applying step to be comparable to a diffusion rate of another impurity (inherent for impurities of higher atomic weight such as As and Sb whose diffusion rate is slower than that of B) in column 6, lines 31 – 35 and in column 8, lines 1 – 12.

Regarding claim 2, Guldi teaches the structure on said surface of said semiconductor material is a gate structure of a field effect transistor with reference to Fig. 5.

Regarding claim 3, Guldi teaches the boundary is defined by a sidewall of said gate structure with reference to Fig. 5.

Regarding claims 4 and 5, Guldi teaches the sidewall is an offset spacer and said sidewall is a source/drain spacer with reference to Fig. 5.

Regarding claim 6, Guldi teaches the boundary is defined by a gate electrode of said gate structure with reference to Fig. 5.

Regarding claim 14, Guldi teaches an intermediate structure for formation of a semiconductor device, said intermediate structure comprising

- a body of semiconductor material including respective regions implanted with boron and arsenic impurities,
- a structure on a surface on said body of semiconductor material and forming a boundary, and
- a stressed film extending over said structure and said boundary, wherein when said intermediate structure is annealed to activate said boron and arsenic impurities, a diffusion rate of said boron impurities is selectively modified in both lateral and vertical directions in a region of said semiconductor material adjacent to said boundary_ to be comparable to a diffusion rate of another impurity as was

described earlier in rejecting claim 1 with references to Figs. 1 – 5 in columns 5 – 8 and especially in column 8, lines 1 – 12.

Regarding claims 15 – 18, Guldi teaches the limitations of these claims as were described earlier in rejecting claims 2 – 5.

Regarding claim 20, Guldi teaches a pFET including

- a source/drain region formed by implantation with boron, and
- an extension region formed by implantation with boron, wherein a boron concentration profile of said extension in a lateral direction differs from a boron concentration in a vertical direction with reference to Figs 1 – 3 and 5 in discussions in between columns 5 – 8 as was described earlier in rejecting claims 1 and 14.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 7 – 12 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Guldi, US 5,525,529 in view of Ahmad, US 6,159,813.

Regarding claim 7, Guldi teaches the steps of implanting extension impurities, implanting source/drain impurities, but fails to teach implanting halo impurities.

Ahmad teaches implanting halo impurities with reference to Fig. 9 for the benefit of optimizing the concentration of p –type charge carriers in column 4, lines 15 – 20.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Guildi and implant halo impurities for the benefit of optimizing the concentration of p –type charge carriers as taught by Ahmad in column 4, lines 15 – 20.

Regarding claim 8, Guldi in view of Ahmad teaches a plurality of said structures are provided on said surface of said semiconductor material, but fails to teach the step of removing said stressed film from a selected said structure prior to said annealing step,

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Guildi in view of Ahmad and remove said stressed film from a selected said structure prior to said annealing step so that the gate top and the source and drain regions can be silicided for lowering resistivity.

Regarding claim 9, Guldi teaches plurality of structures include gate structures of pFETs and nFETs with reference to Figs. 1 – 3.

Regarding claims 10 – 12, Guldi teaches these limitations as were described earlier in rejecting claims 3 – 5.

Regarding claim 19, Guldi teaches an integrated circuit comprising a pFET, and an nFET, but fails to teach wherein a boron diffusion concentration profile from extension implants in said pFET corresponds to a lower boron diffusion rate than a boron diffusion rate corresponding to a boron diffusion concentration profile from a boron halo implant in said nFET.

Ahmad teaches implanting halo impurities with reference to Fig. 9 for the benefit of optimizing the concentration of p –type charge carriers in column 4, lines 15 – 20.

Therefore, the net effect of annealing after the halo implant will produce a boron diffusion concentration profile from extension implants in said pFET corresponds to a lower boron diffusion rate than a boron diffusion rate corresponding to a boron diffusion concentration profile from a boron halo implant in said nFET.due to the stress effect of the silicon nitride film in Guldi's device.

7. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Guldi, US 5,525,529 in view of Yeo, US 6,882,025.

Guldi teaches the stressed film, but fails to teach the film is a tensile film.

Yeo teaches the deposited silicon nitride film is associated with intrinsic tensile stress in column 4, lines 59 – 61.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention that the silicon nitride film is associated with intrinsic tensile stress as taught by Yeo in column 4, lines 59 – 61.

Response to Arguments

8. Applicant's arguments filed July 8, 2009 have been fully considered but they are not persuasive due to the following reasons. The Applicant cites various phrases such as "localized application of compressive stress" (see paragraph 2, page 12) and then goes on to mention that Guldi does not mention the term "compressive". The Examiner notes that none of the claims in question has limitation with the term "compressive" or "localized." Therefore, the argument that Guldi does not mention the term compressive stress is not at all persuasive.

The Applicant, however, agrees that Guldi teaches applying films of different chemical compositions (see paragraph 2, page 12). It is well known that silicon nitride films have intrinsic tensile stress(see explanation later). Guldi also teaches that silicon deficient nitride films can apply stress to retard diffusion in column 8, lines 1 – 12. Thus, films deposited over the gate with different chemical composition can, in fact, apply stress due to their chemical composition to the substrate region near the gates explained above in the rejection of claims. Therefore, Applicant's allegation that Guldi teaches away from the claimed invention is not persuasive. Similarly, Applicant's

allegation that Guldi's control of diffusion does not appear to be selective (paragraph 1, page 13) is not persuasive. First, the term, "selectivity ", is used only as a preamble in claim 1, which cannot, in the present case, be given any patentable weight. Second, Guldi teaches that the blocking layer can be selectively placed on a source or a drain region so that the diffusion of impurity such as B is only controlled in one of the junctions thereby satisfying the claim language of controlling the diffusion rate of one impurity to match the diffusion of another impurity, which can be in a different part of the device. Thus, Guldi's teachings satisfy the term "selective modification" in claim 14.

It is also immaterial whether the stress appears before annealing or after annealing (see paragraph 1, page 13) since the claimed steps use the term "including" in the preamble. Furthermore, it is a common practice in the semiconductor industry to anneal deposited film for densification and also to homogenize the stress distribution.

Similar argument can be expressed regarding the limitations of claim 19, since the two implants are at two different regions and the diffusion is controlled by the stressed/ compositionally different film in only one region.

Regarding claim 20 (paragraph 3, page 14), the claim language is such that the concentration profile of boron is different in the lateral direction than that in the vertical direction and do not, in fact, require any stressed film (see the Applicant's Fig. 3A). Thus, the argument that Guldi does not teach the limitations of this claim is not persuasive. Guldi teaches the limitation in column 6, lines 30 – 35.

The argument regarding Ahmad is also not relevant since the claim language is silent about the thickness of spacers.

Regarding Yeo (paragraph 2, page 15), the Applicant argues that that Yeo's teaching is not relevant because the silicon nitride lines trench isolation structures. This is also not persuasive since the stress is "intrinsic" and therefore will appear to be in tension on any structure since the stress is generated due to composition.

The Examiner, therefore, maintains the rejection.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Asok K. Sarkar whose telephone number is 571 272 1970. The examiner can normally be reached on Monday - Friday (9 AM- 6 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kiesha L. Rose can be reached on 571 272 1844. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Asok K. Sarkar/
Primary Examiner, Art Unit 2891
September 16, 2009